In-Pixel Computing for the Extreme-Edge

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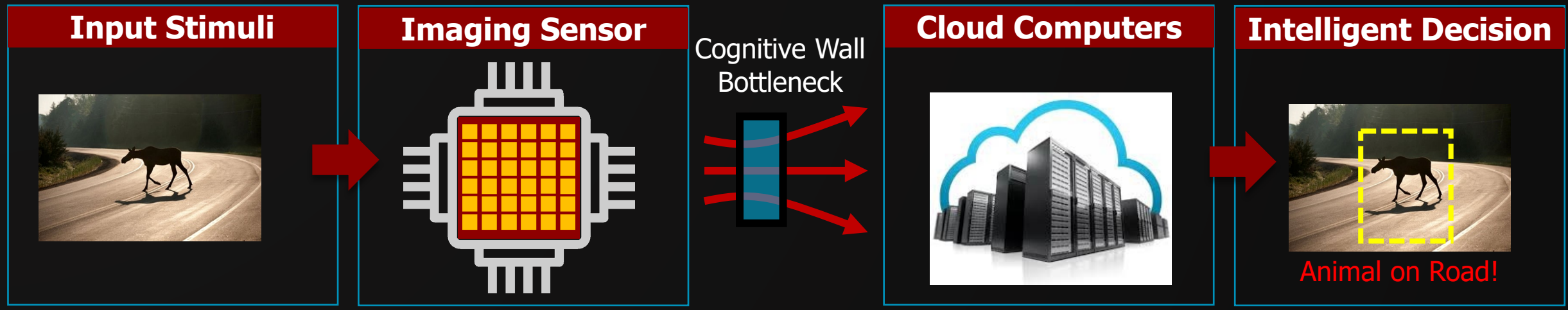
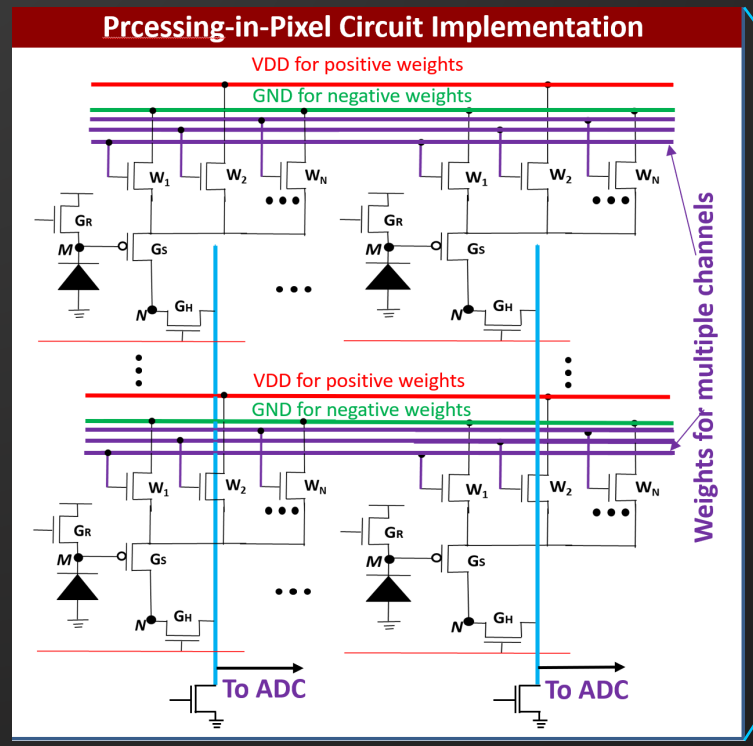
State of the art vision sensors are SWAP constrained

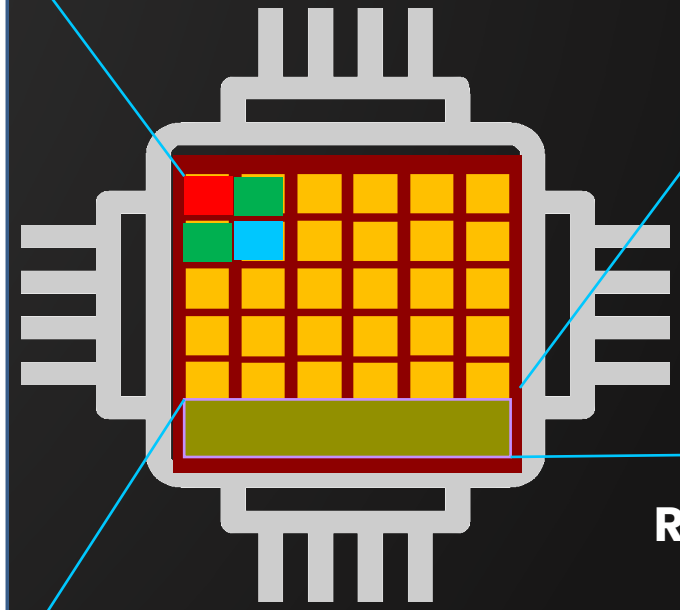


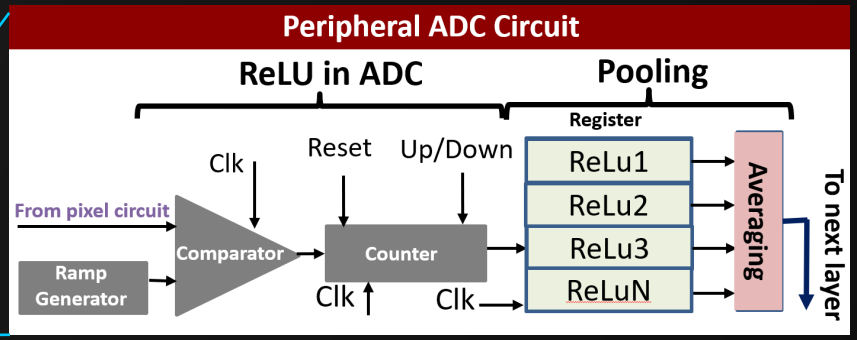
The segregation of 'Sensing', 'Memory' and 'Compute' creates Energy, Throughput, and Bandwidth Bottleneck.

In-Pixel Technology efficiently Balances Compute Energy, Data Movement, and Accuracy



Massively parallel in-pixel Analog Multibit Convolution Operation

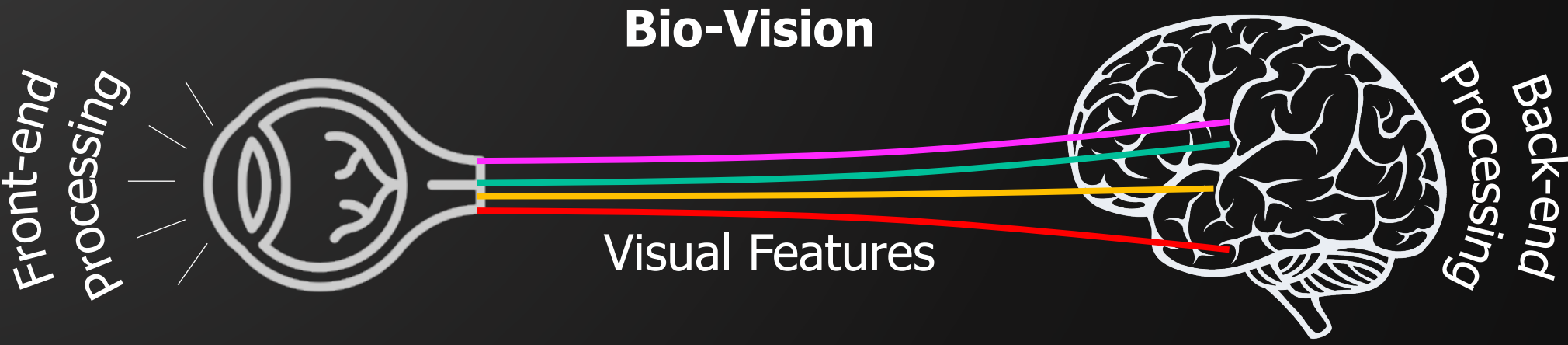




Re-purposed Column Parallel ADCs

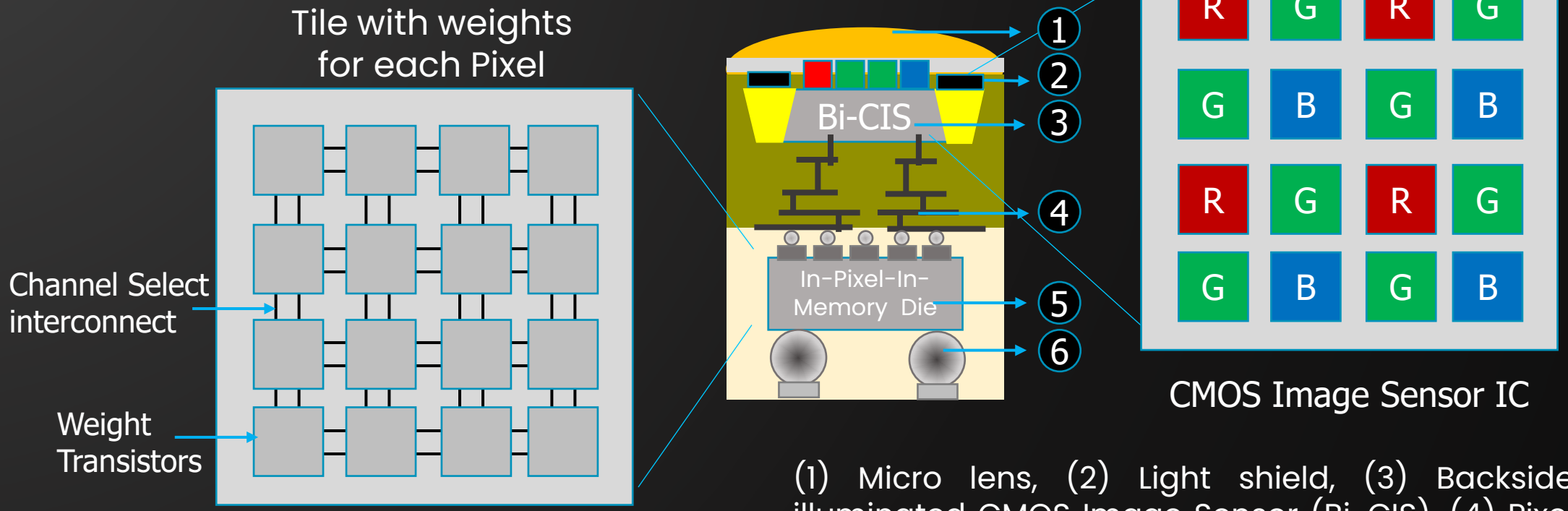
Hardware maps all the computational aspects of the first few layers of CNN inside sensor, minimizing data transfer for Neuron-Ready Processing

In-Pixel Compute Analogy with Bio-vision



In-PIXEL Processing is a Bio inspired solutions to address the sensing-computing bottleneck

Representative illustration of a stacked in-pixel hardware design

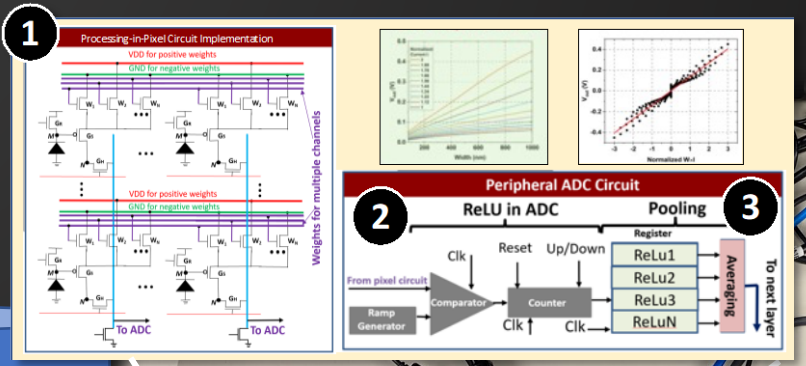


(1) Micro lens, (2) Light shield, (3) Backside illuminated CMOS Image Sensor (Bi-CIS), (4) Pixel isolation (5) Backend of line of the Bi-CIS, (6) in-Pixel Memory tile

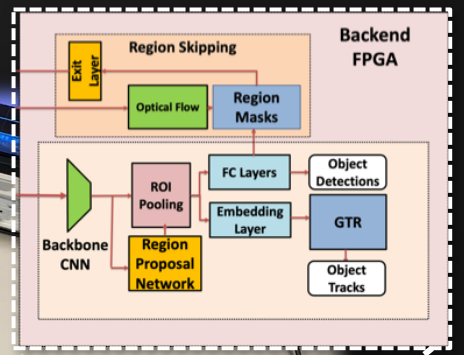
3D Heterogeneous Integration: Achieving high-density pixels with State-of-the-art performance through high volume manufacturing

In-Pixel Experimental Demonstration

In-Pixel Frontend Circuit Emulation



In-Pixel Backend FPGA

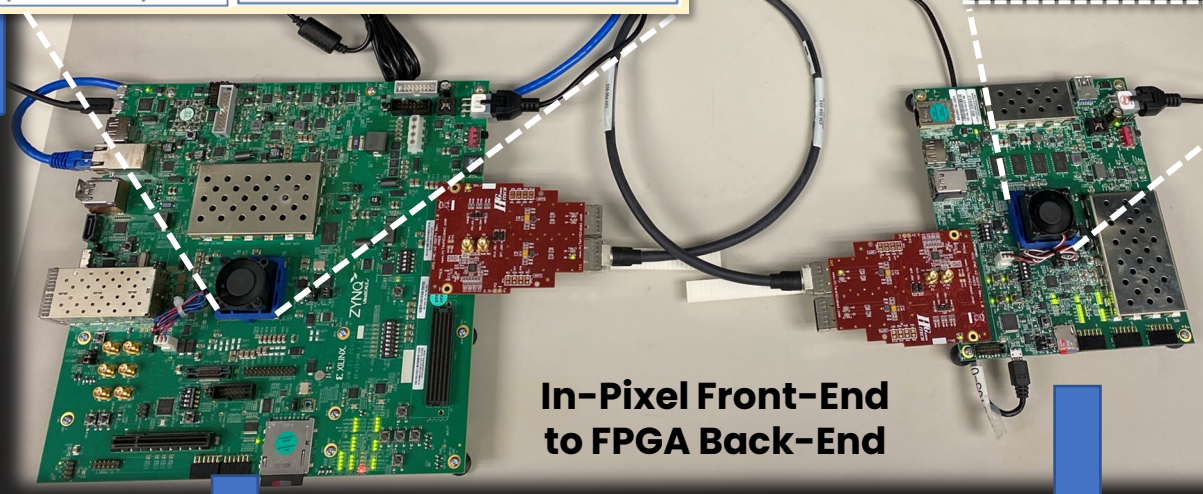


Output Video

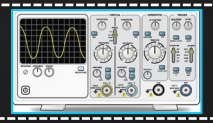
Input Dataset

Front-end Sensor

1. Curve Fitting
2. Quantized ReLU
3. Batch Norm.
4. Pooling

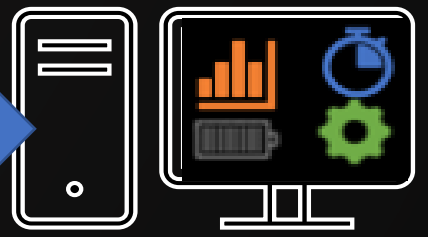


In-Pixel Front-End to FPGA Back-End



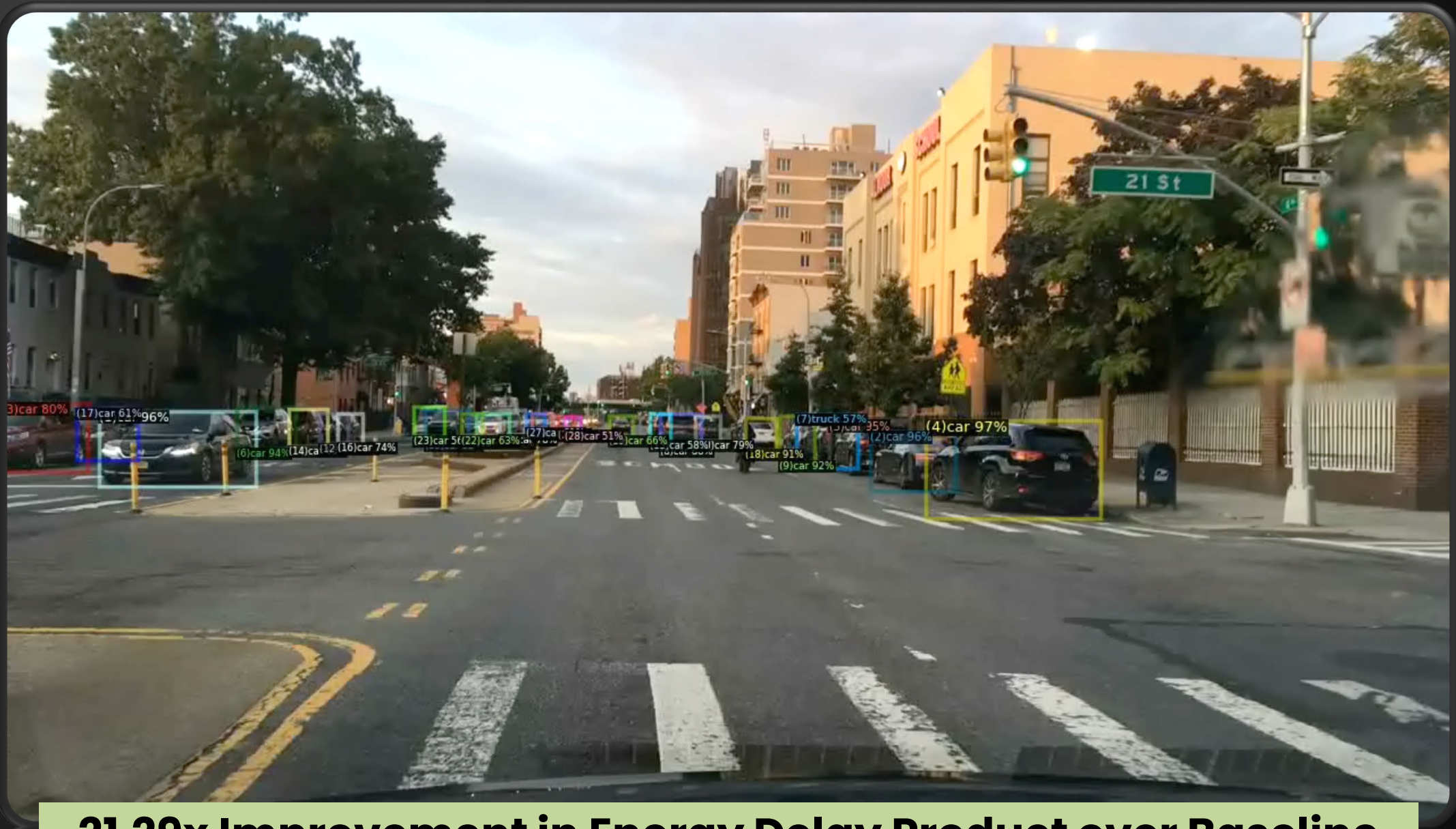
In-Pixel Power, Performance & Area

Results



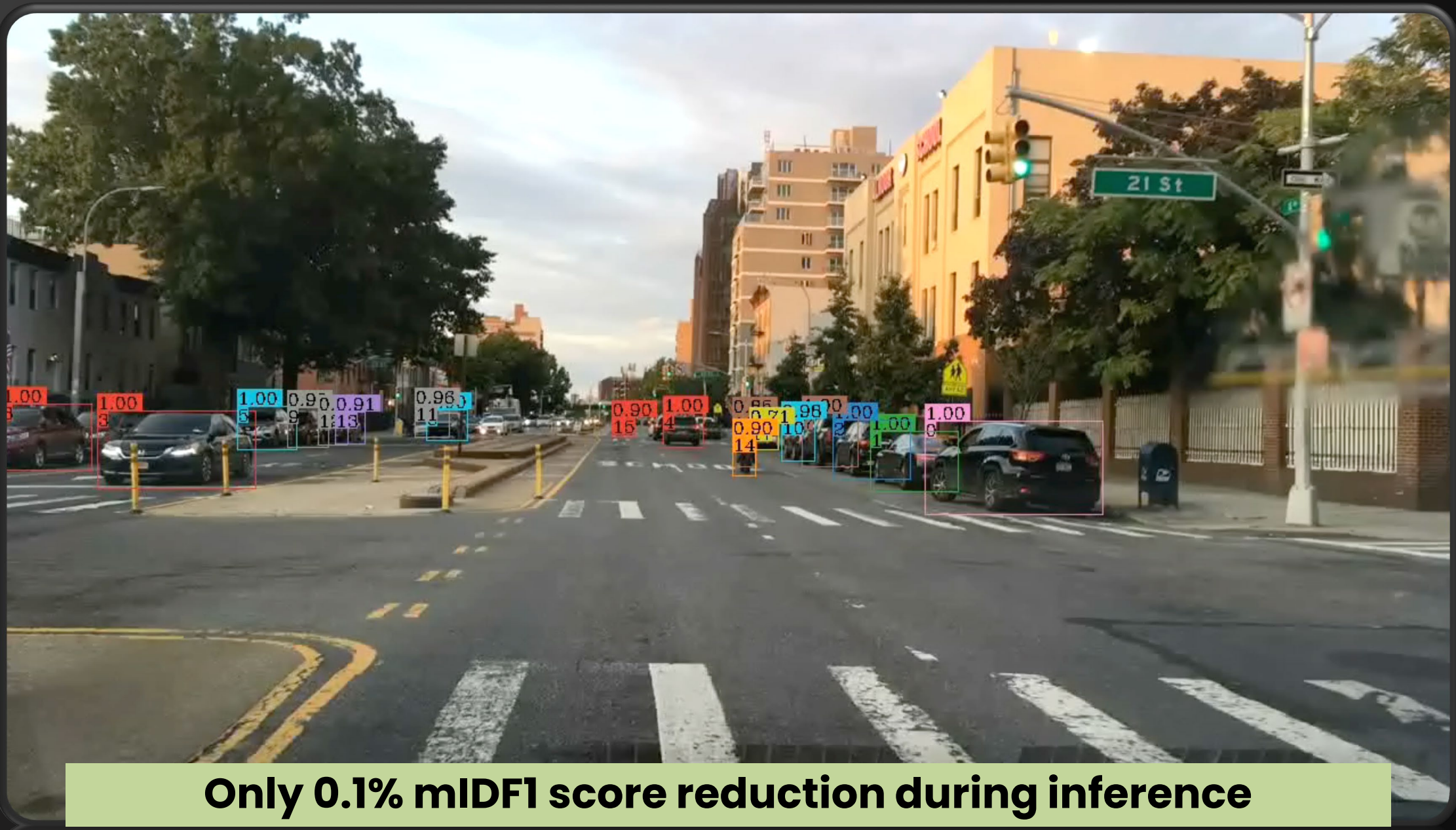
Baseline Performance

In-Pixel Accelerated Global Tracking Transformers



21.29x Improvement in Energy Delay Product over Baseline

In-Pixel Accelerated with 5% Noise



Only 0.1% mIDF1 score reduction during inference

In-Pixel Intelligent Frame Skipping

Baseline

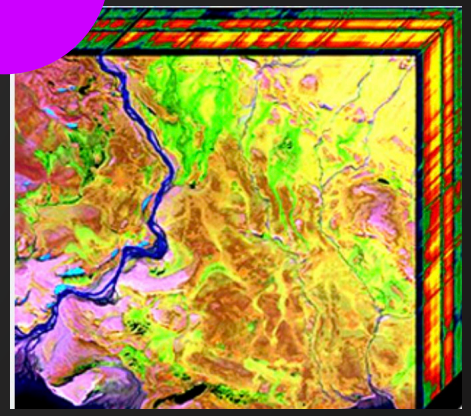
In-Pixel Intelligent Frame Skipping

13.3x Speedup with In-Pixel Intelligent Frame Skipping

Significant bandwidth reduction at SOTA accuracy

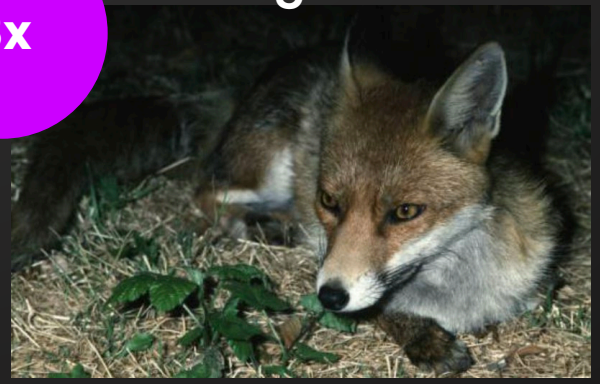
12x Visual Tiny ML

10x Hyperspectral Imaging

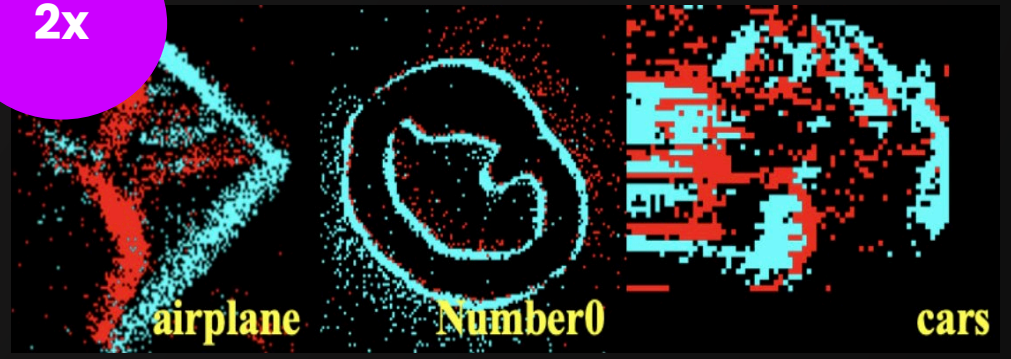


13x Multi-object Tracking

8x Complex Image Recognition



2x Event-Driven Neuromorphic Tasks (DVS Cameras)



In-Pixel processing enables a wide range of SWaP constrained complex Machine Learning tasks at the Extreme-Edge

In-PIXELS Team Members

Frontend In-Pixel design

Dr. Ajey Jacob (PI)	Dr. Akhilesh Jaiswal (Co-PI)
Hardware Demonstration	In-Pixel Circuit Architecture

Backend Neural Network design

Dr. Peter Beerel (Co-PI)	Dr. Wael Abd-Almageed (Significant Contributor)	Dr. Andrew Schmidt (Significant Contributor)
NN Algorithm-Hardware Co-design	Backend Multi-object Detection and Tracking	FPGA Implementation and Demonstration

THANK YOU